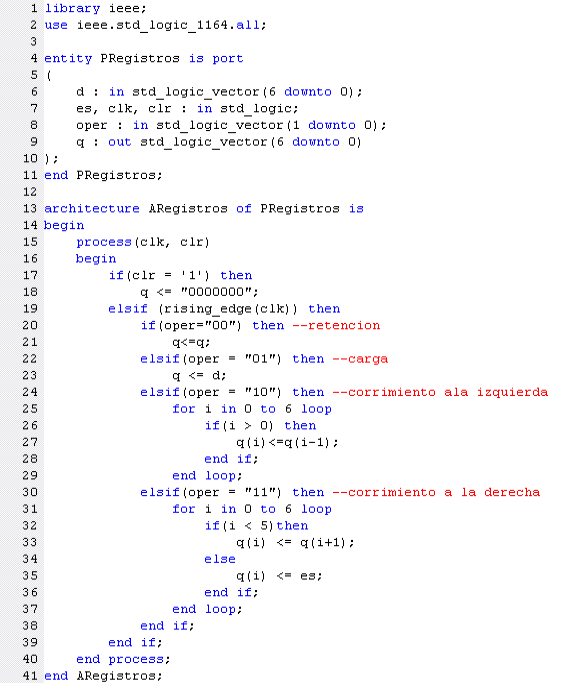
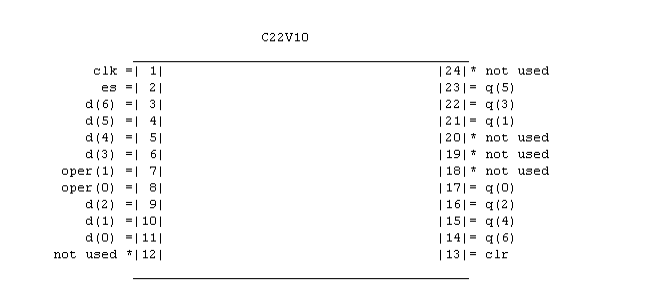
Córdova Pichardo Francisco Uziel

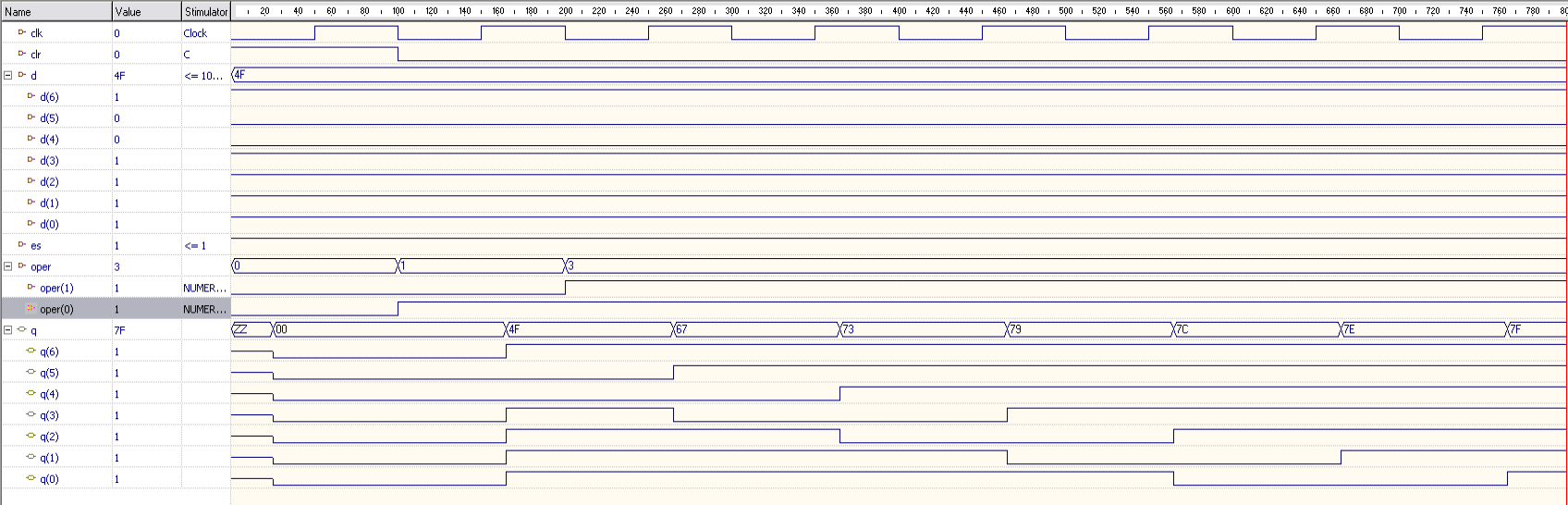
Practica 3





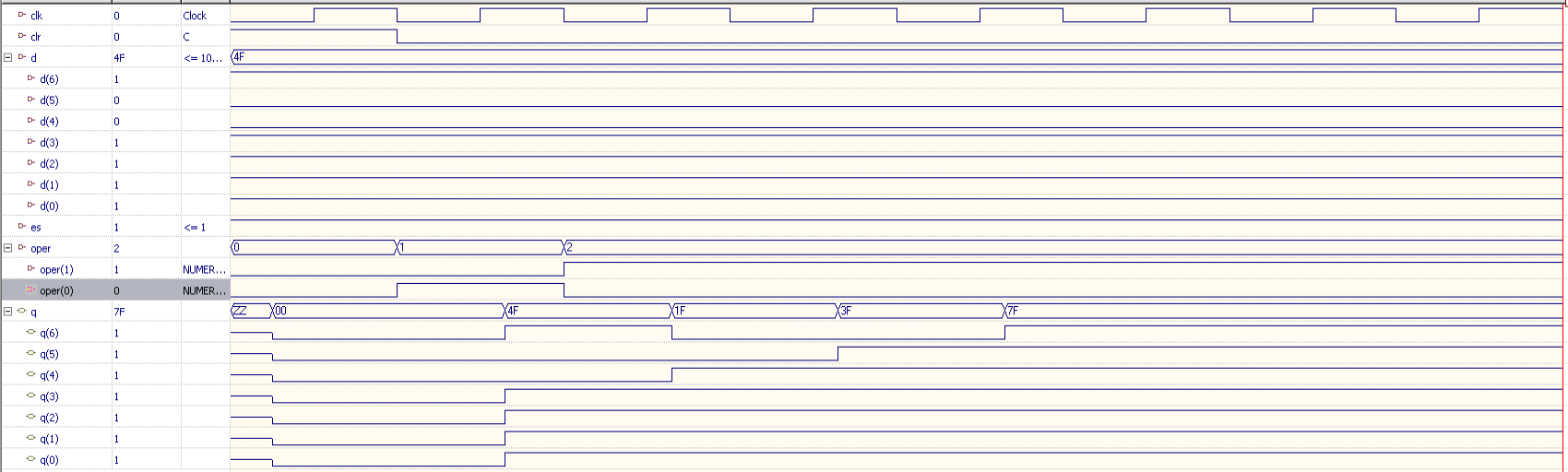
Entrada d= 1001111

Corrimiento a la derecha



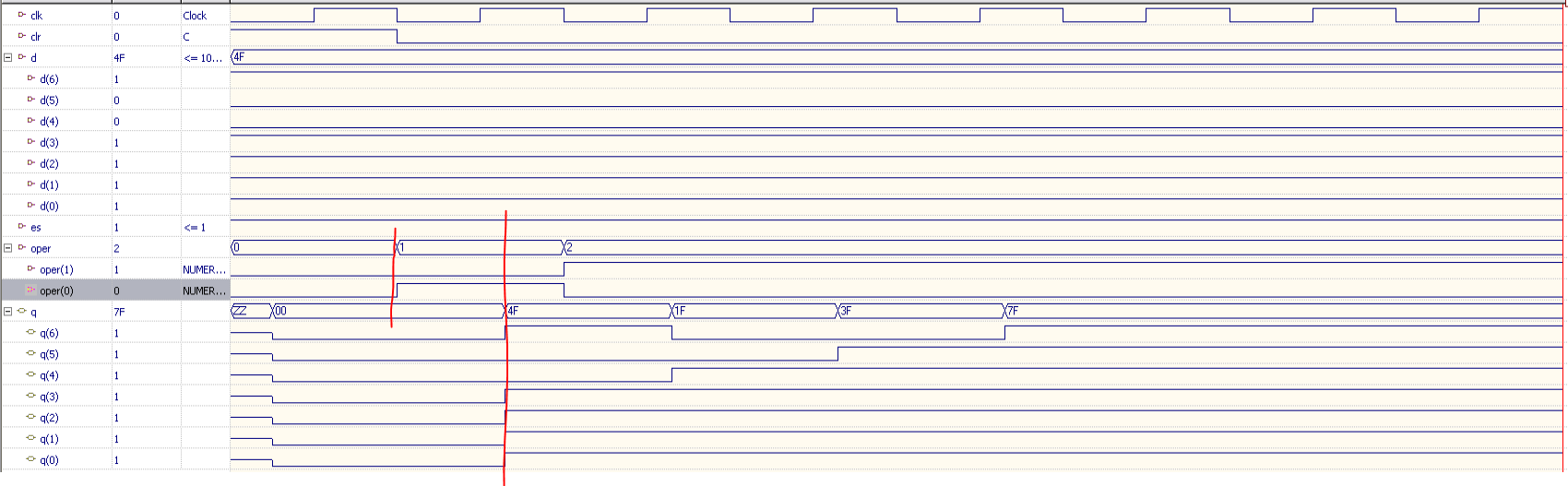
Salida q=1100111, 1100111, 1110011, 1111001, 1111100, 1111110, 1111111

Corrimiento a la izquierda

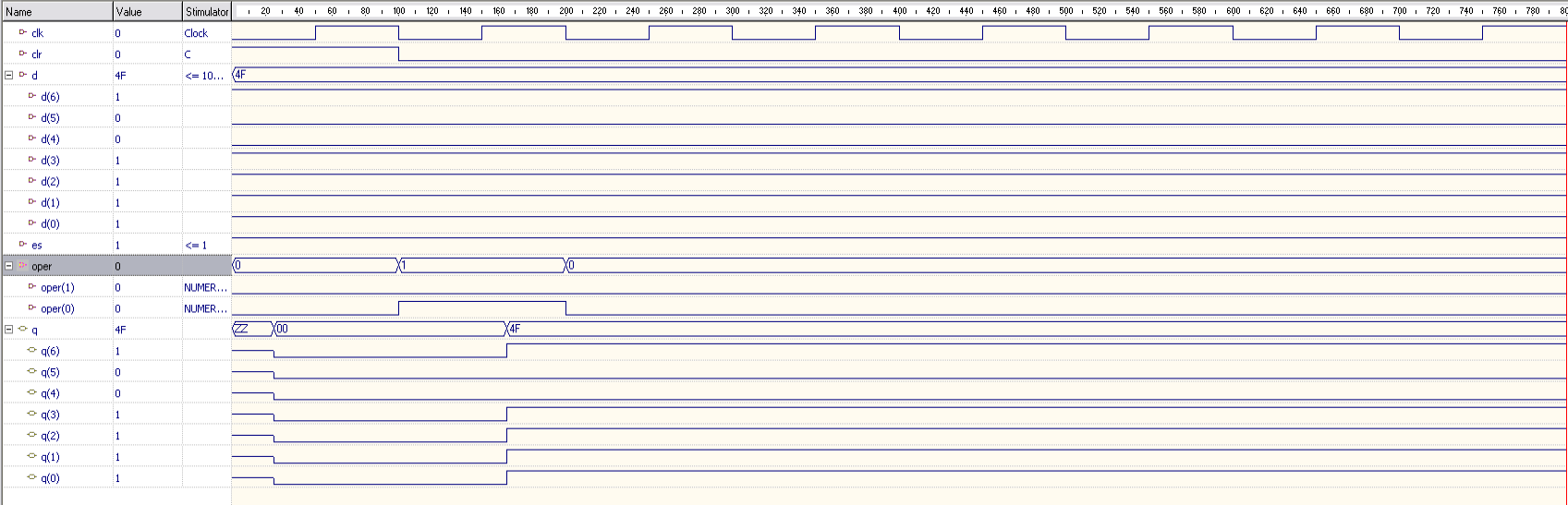
Entrada d=1001111 

Salida q=1001111, 0011111, 0111111, 111111

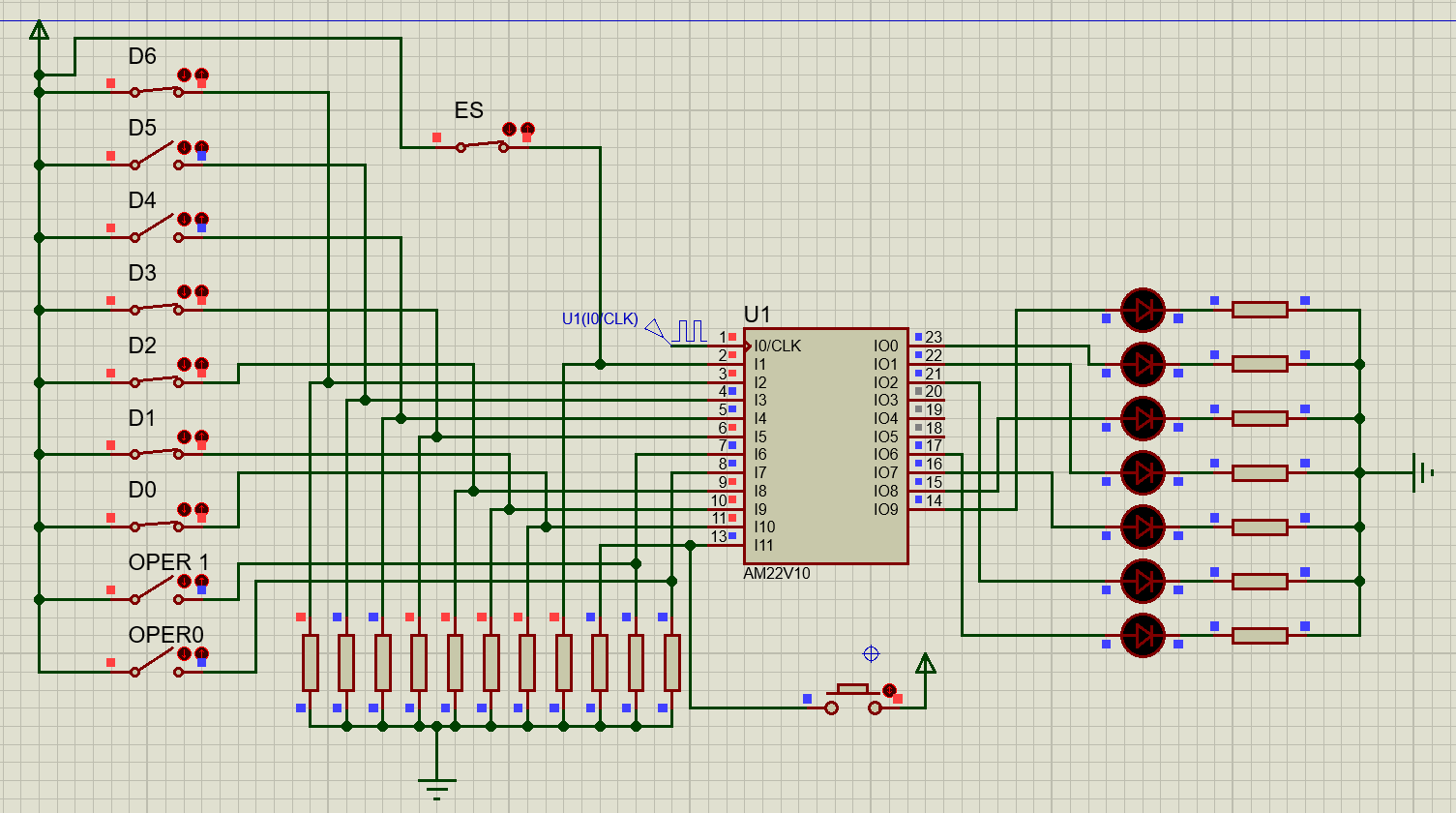
La carga de bits se ve en este punto en ambas simulaciones en el flanco de ascenso



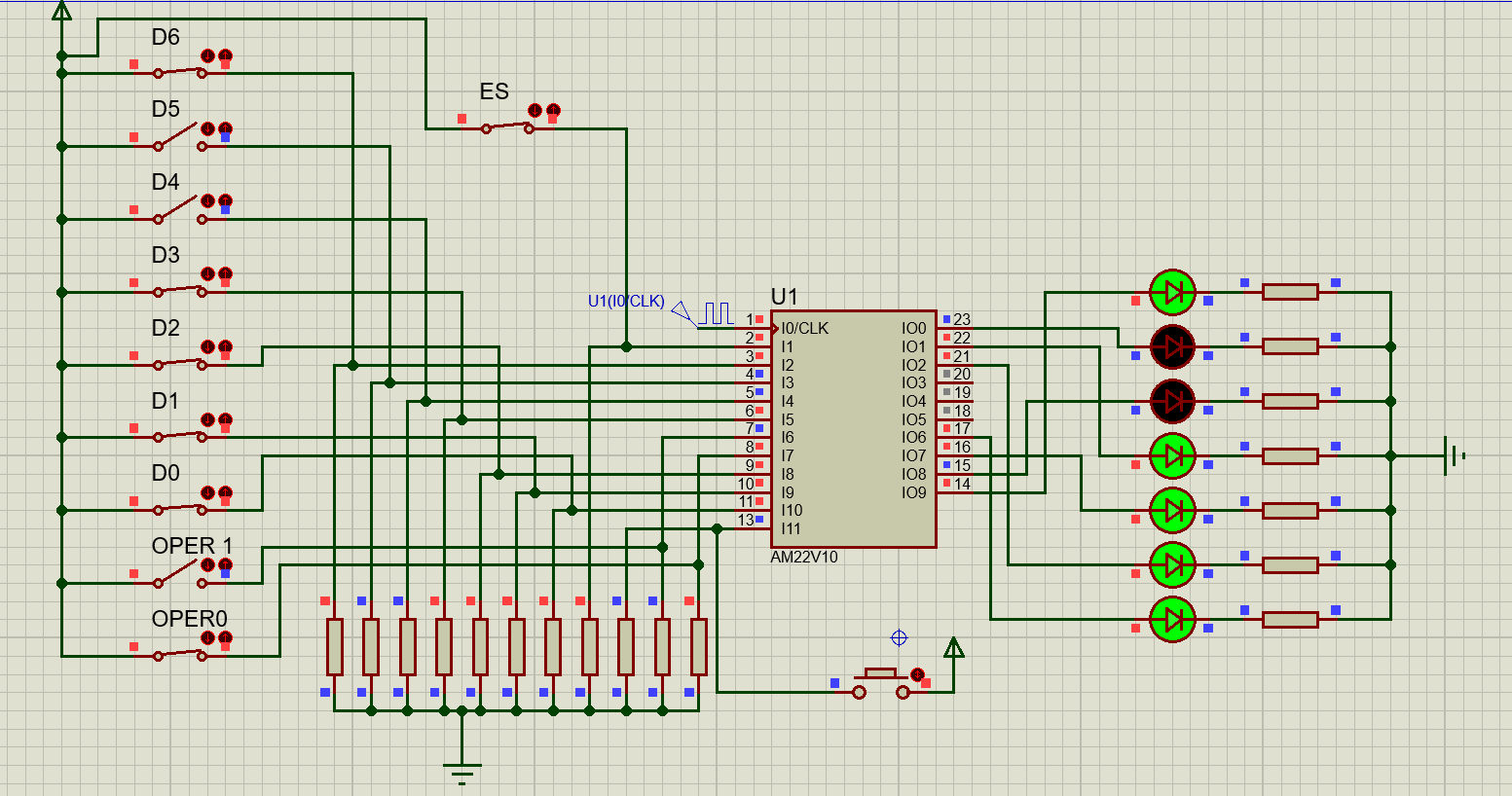
Retención de bits



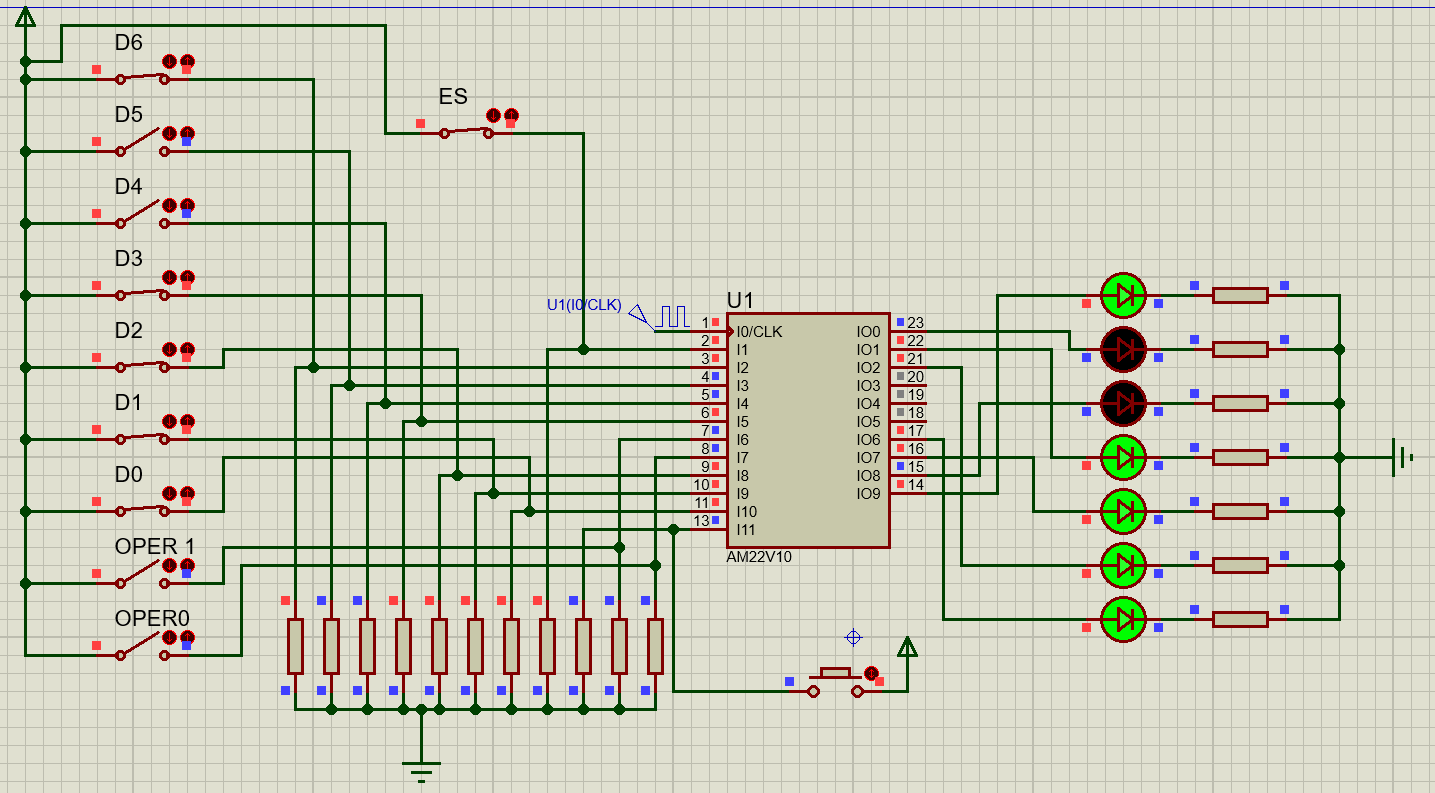
Simulación proteus



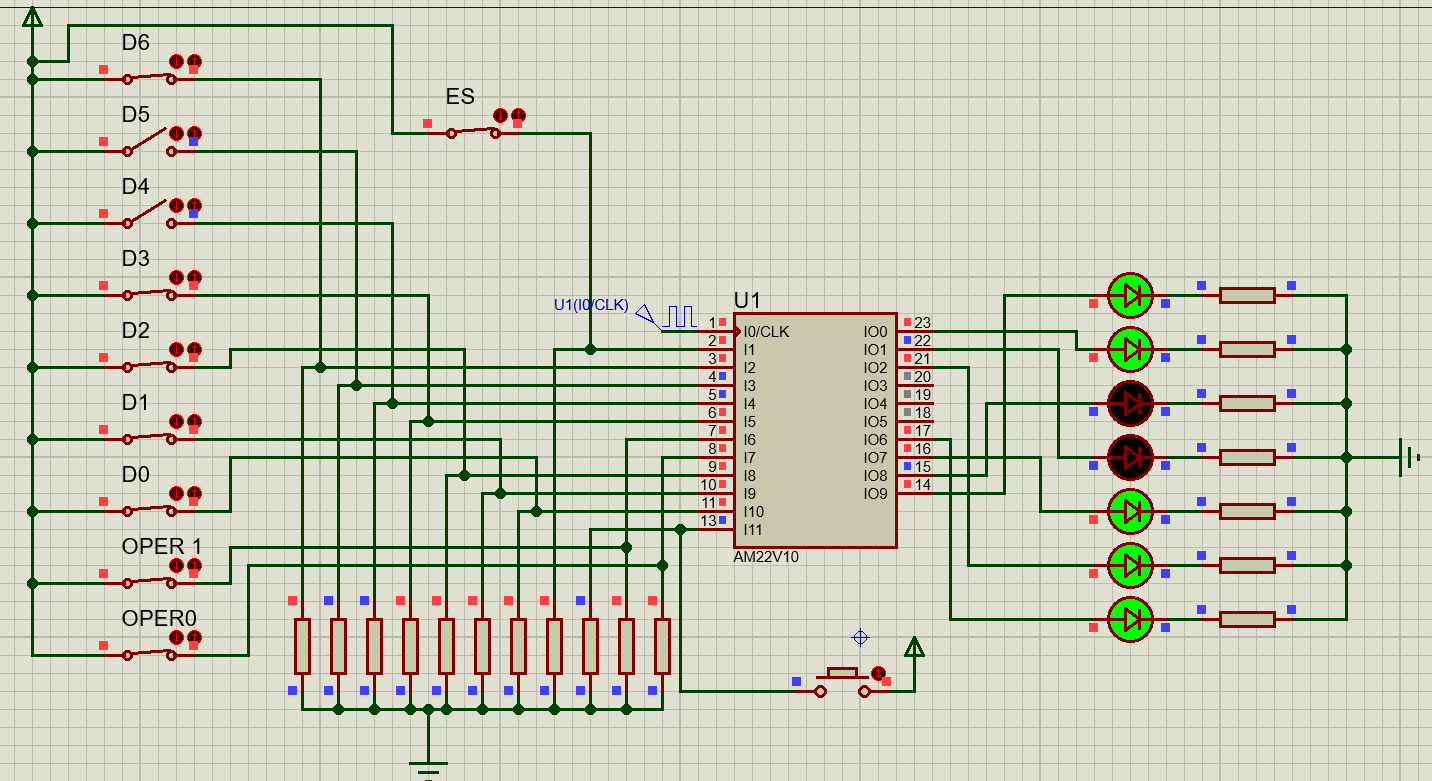
Carga de bits

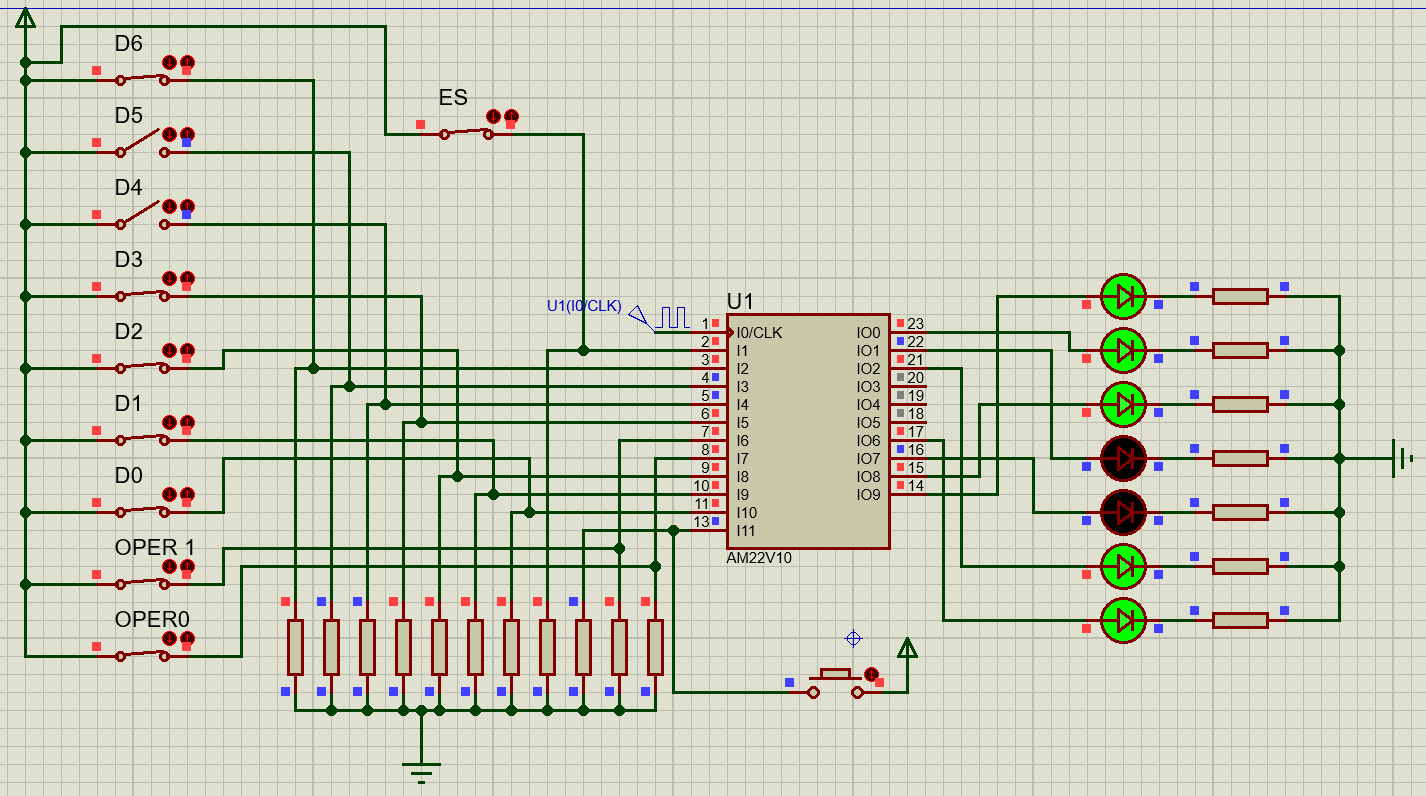


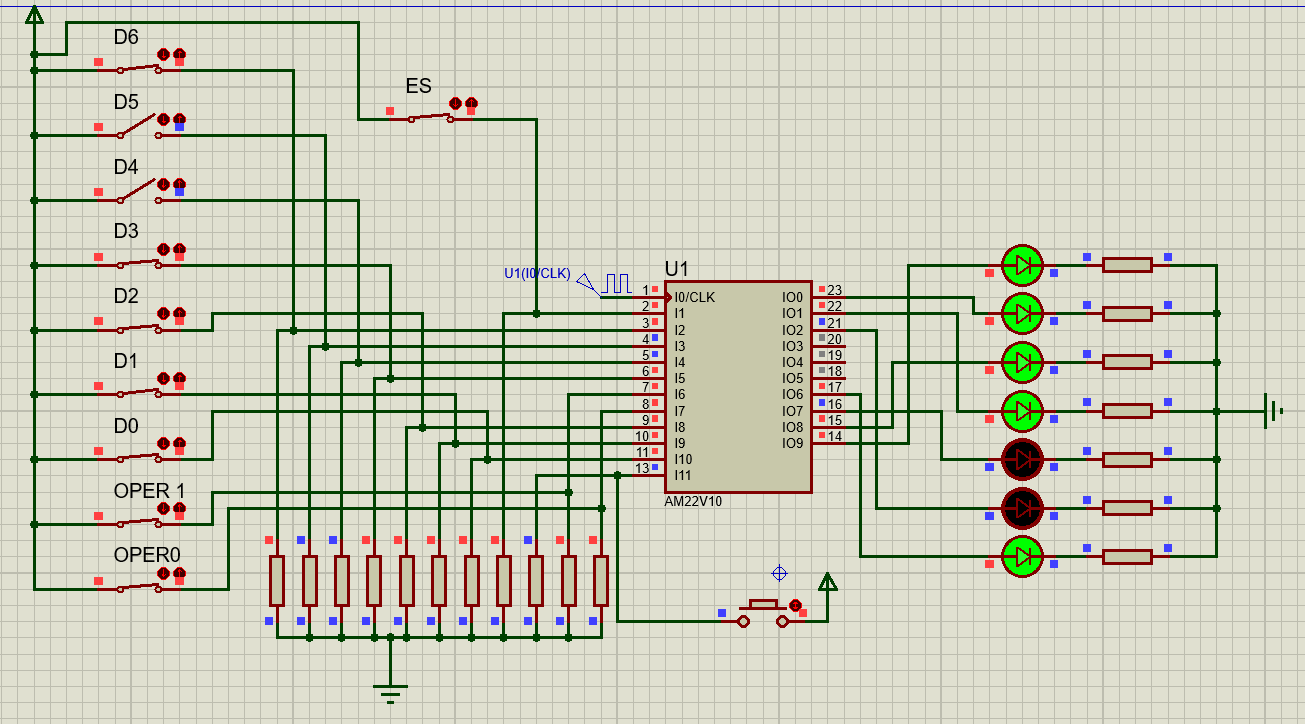
Retención de bits

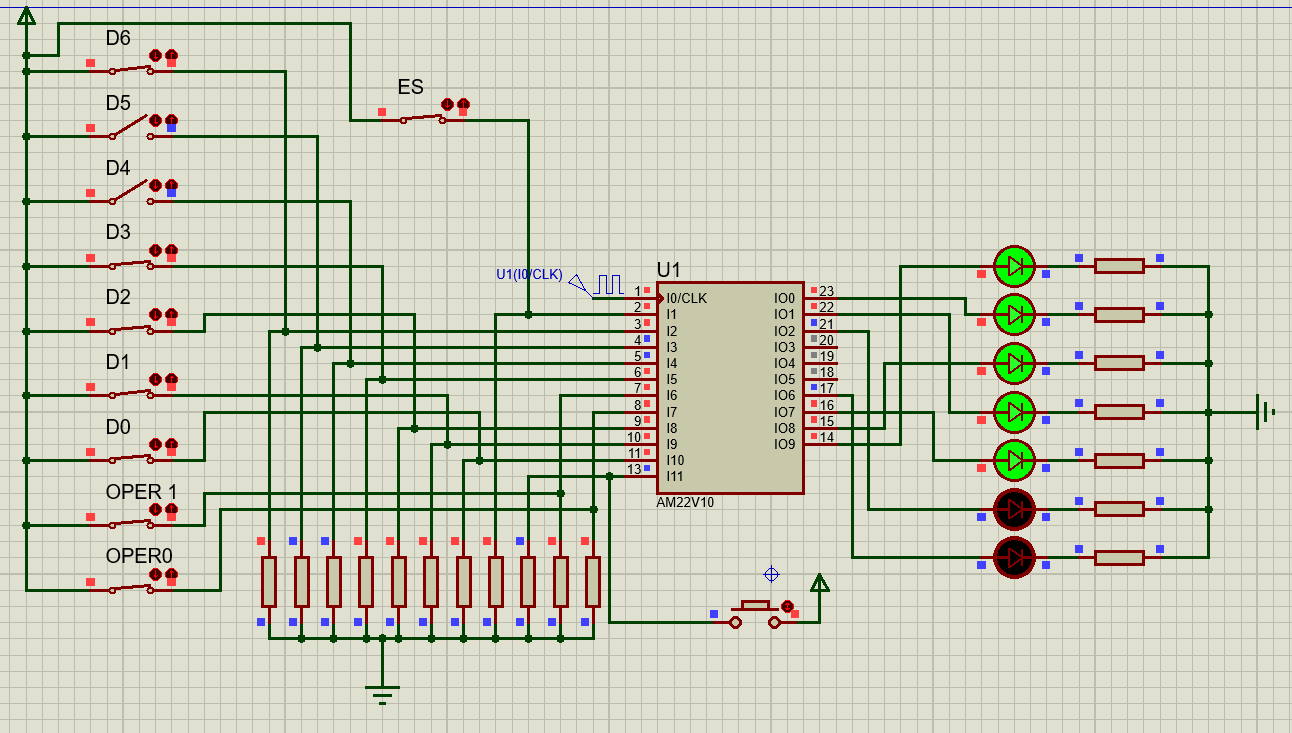


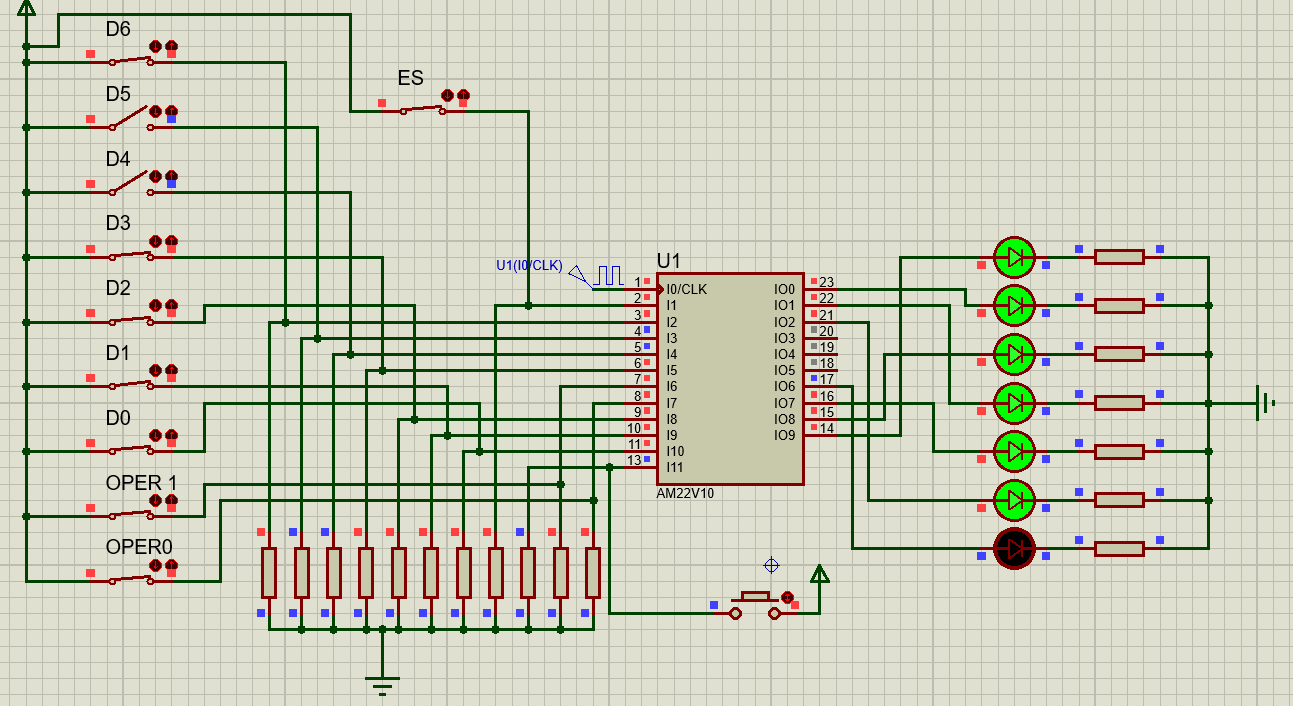
Corrimiento a la derecha

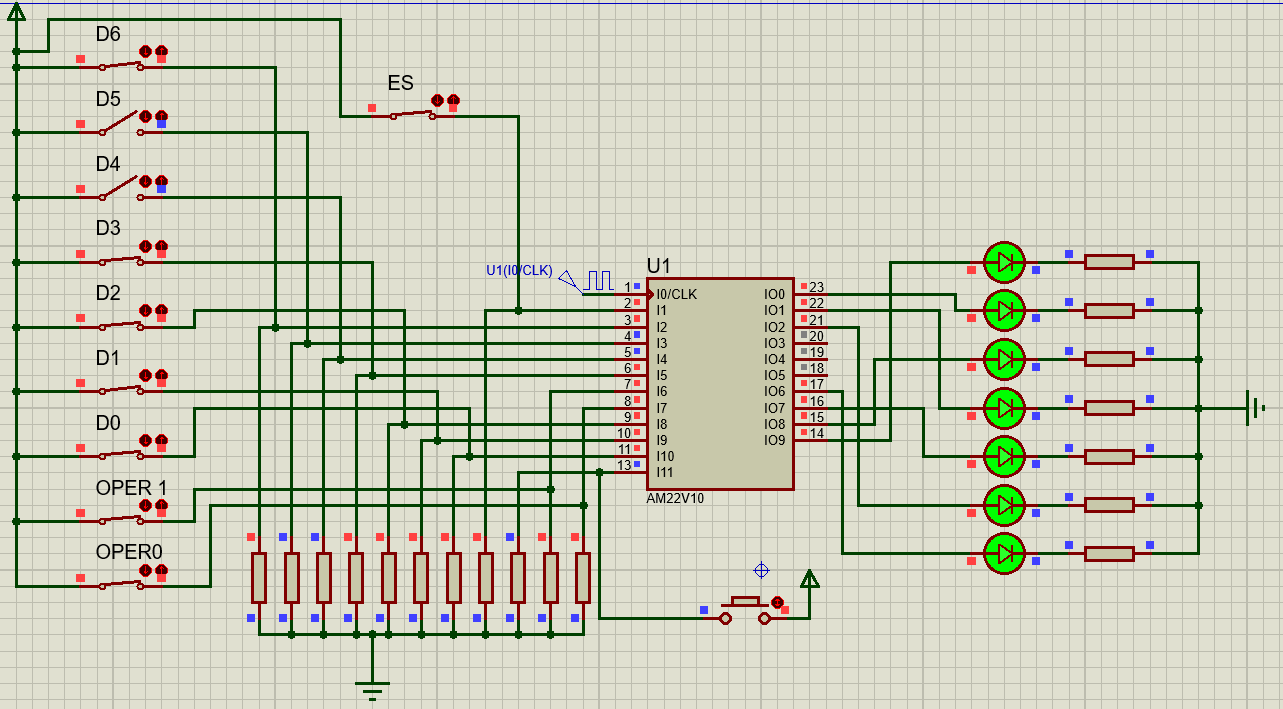












Corrimiento a la izquierda

